REMARKS

In accordance with the foregoing, claim 1 is amended. Claims 1-5 and 11 are pending and under consideration.

REJECTION UNDER 35 U.S.C. §102

Claims 1-5 and 11 are rejected under 35 U.S.C. 102(a) as allegedly being anticipated by the applicant's prior art (AAPA).

Claim 1 is amended herewith to clarify the claimed subject matter. The claim amendments are fully supported by the originally filed specification, for example, FIG. 4 and page 12, line 23 to page 13, line 28.

The outstanding Office Action (as the previous Office Action did) groups many claims (e.g. 1-5 and 11) in a single "rejection" and, as a result, fails to address specific recitations of the claims and respond to Applicants arguments. Applicants respectfully submit that the Office Action does not meet the standard set forth in 37 C.F.R. 1.104 (c)(2). MPEP 2143.03, which states "[all] words in a claim must be considered in judging the patentability of that claim against the prior art," likewise is not satisfied.

The Office Action alleges that "Figure 1 of AAPA illustrates [...] first data path (e.g. elements13-12-2) and second data path (e.g. elements 15-14-4) provided to connect the decoder 16 to the input memories (3, 5)" (see the "Response to Arguments" section, on page 3 of the outstanding Office Action).

Although the video data may flow from the decoder 16 via the video output memory 13, the video output interface 12, and the video input interface 2 to the video input memory 3, Applicants believe that this manner of transferring data is not "a first data path provided **to connect the decoder to the video input memory**" as recited in claim 1. Similarly, although the audio data may flow from the decoder 16 via the audio output memory 15, the audio output interface 14, and the audio input interface 4 to the audio input memory 5, to the audio input memory 5 is not "a second data path provided **to connect the decoder to the audio input memory**."

Additionally, in view of claim 1 amendments, FIG. 1 does not anticipate or render obvious "a video input memory storing video data which [...] is received internally from the decoder" and "an audio input memory storing audio data which [...] is received internally from the decoder."

Furthermore, prior art does not teach or suggest "first data path provided to connect the decoder underline directly to the video input memory, when the transcoding is performed" and "a second data path provided to connect the decoder underline directly to the audio input memory, when the transcoding is performed."

In a non-limiting embodiment of claim 1 illustrated in FIG. 3, a first data path 17 connects **directly** the decoder 16 to the video input memory 3, when the coded stream of the first format is transcoded to generate a second stream of a second format. A second data path 18 connects **directly** the decoder 16 to the audio input memory 5 therein, when the transcoding is performed. As explained in the specification, the video data received directly from the decoder is stored in the video input memory via the first path in order to be delivered to the encoder (instead of the video data supplied from the video output interface). The audio data received internally directly from the decoder is stored in the audio input memory via the second data path in order to be delivered to the encoder (instead of the audio data received from the audio output interface). Therefore, the undesirable effects of the control which prevents an underflow or an overflow of the video and/or audio output memory are eliminated.

Claims 2-5 depending from claim 1 are also patentable at least by inheriting patentable features from independent claim 1, but also by reciting additional patentable features. For example, claim 5 recites "a clock generating unit generating a clock signal for circuit components of the data encoding/decoding apparatus wherein the clock signal from the clock generating unit is supplied to each circuit component **without adjusting a phase of the clock signal** based on clock reference information of the coded stream inputted on real time." Although the conventional data encoding/decoding apparatus illustrated in FIG. 1 includes a clock generating unit 8, the clock signal therein is supplied **after being phase adjusted** by the phase adjustment unit 7.

The Office Action does not present arguments for rejecting independent claim 11 separately from the arguments for rejecting claim 1. However, independent claim 11 does not recite the first and second data paths. Applicants asserted in the amendment filed on July 19, 2007 that

> Claim 11 is patentable at least by reciting "a video input memory
> storing the video data received **directly** from the decoder or from a
> source external to the encoding/decoding apparatus" and "an
> audio input memory storing the audio data received **directly** from
> the decoder or from a source external to the encoding/decoding
> apparatus" (emphasis ours).

Receiving video data from the decoder 16 via the video output memory 13, the video output interface 12, and the video input interface 2 to the video input memory 3 is **not receiving directly**. Similarly, receiving audio data from the decoder 16 via the audio output memory 15, the audio output interface 14, and the audio input interface 4 to the audio input memory 5, to the audio input memory 5 is **not receiving directly**. For at least these reasons, independent claim 11 patentably distinguishes over AAPA.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: <u>February 4, 2008</u>   By: _____

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